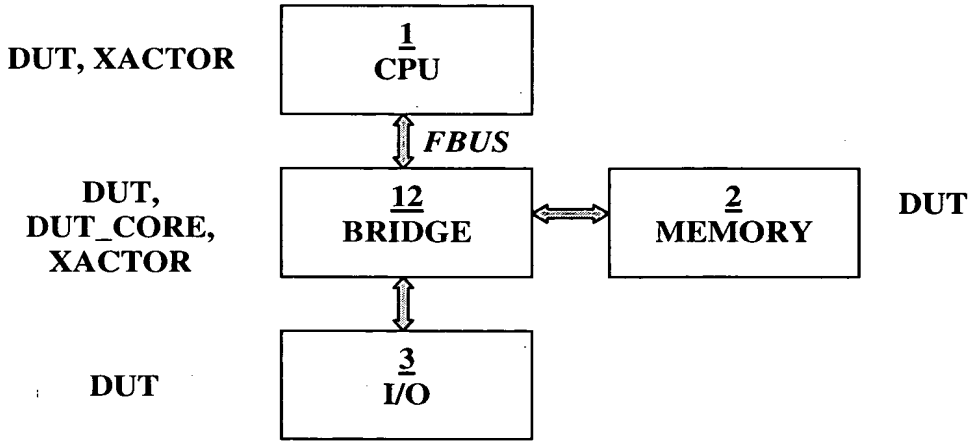


F I G U R E 1

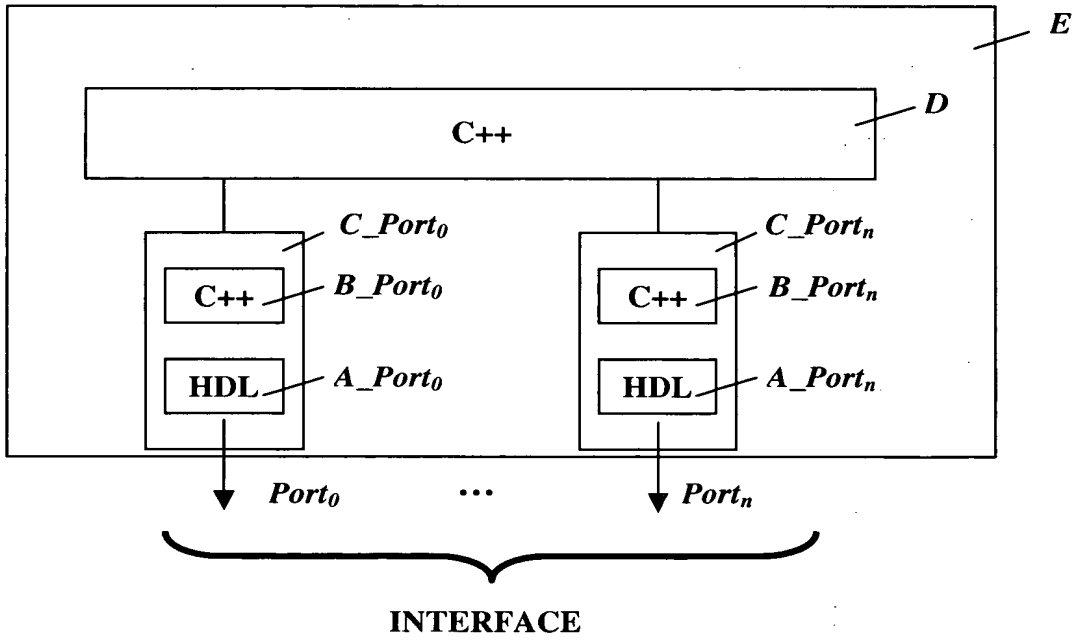
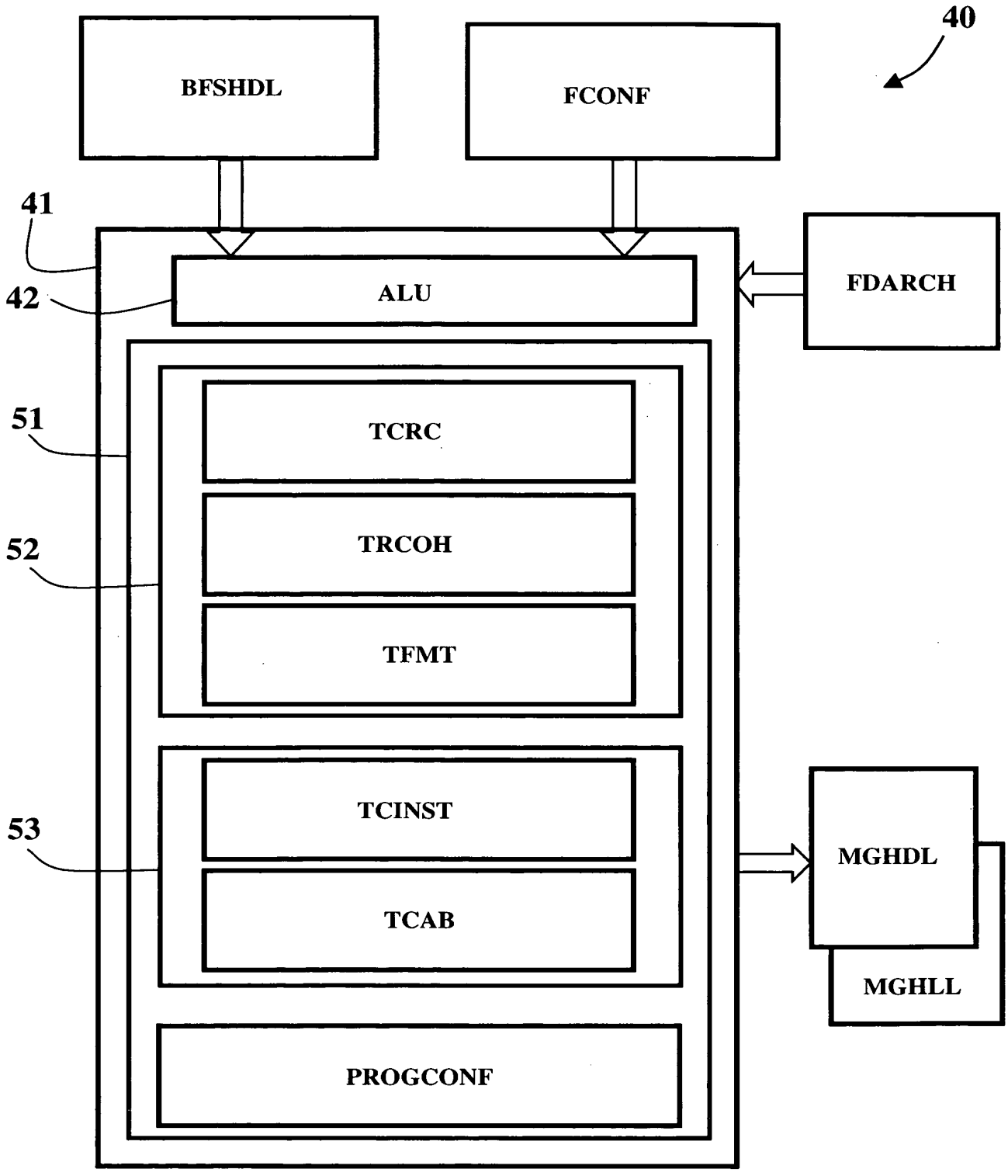


Figure 5 : Generic structure of a C++ Composite Model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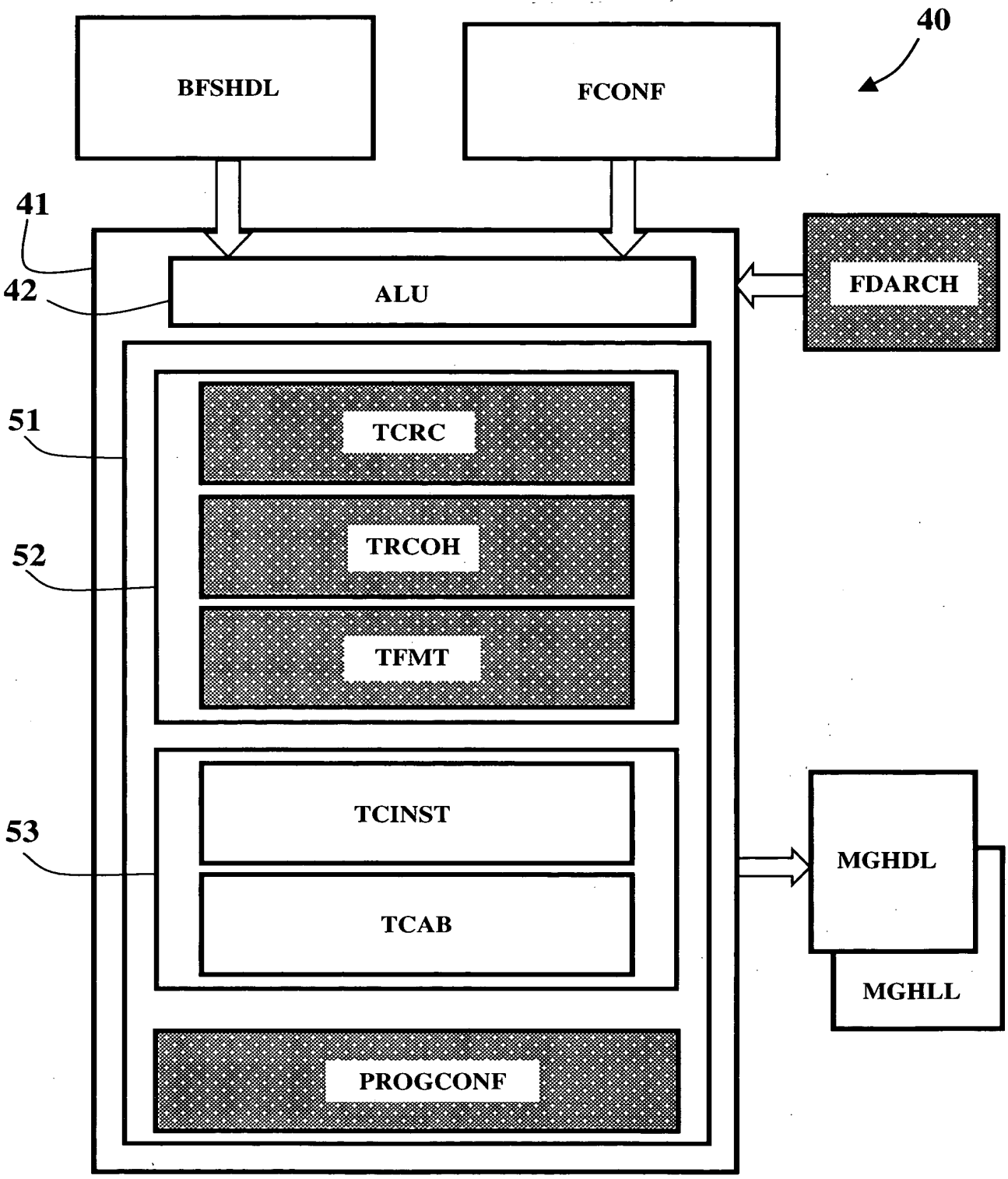
BFSHDL
FCONF
41
42
ALU
FDARCH
51
TCRC
52
TRCOH
TFMT
53
TCINST
TCAB
MGHDL
MGHLL
PROGCONF

FIGURE 2A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TCINST
TCAB
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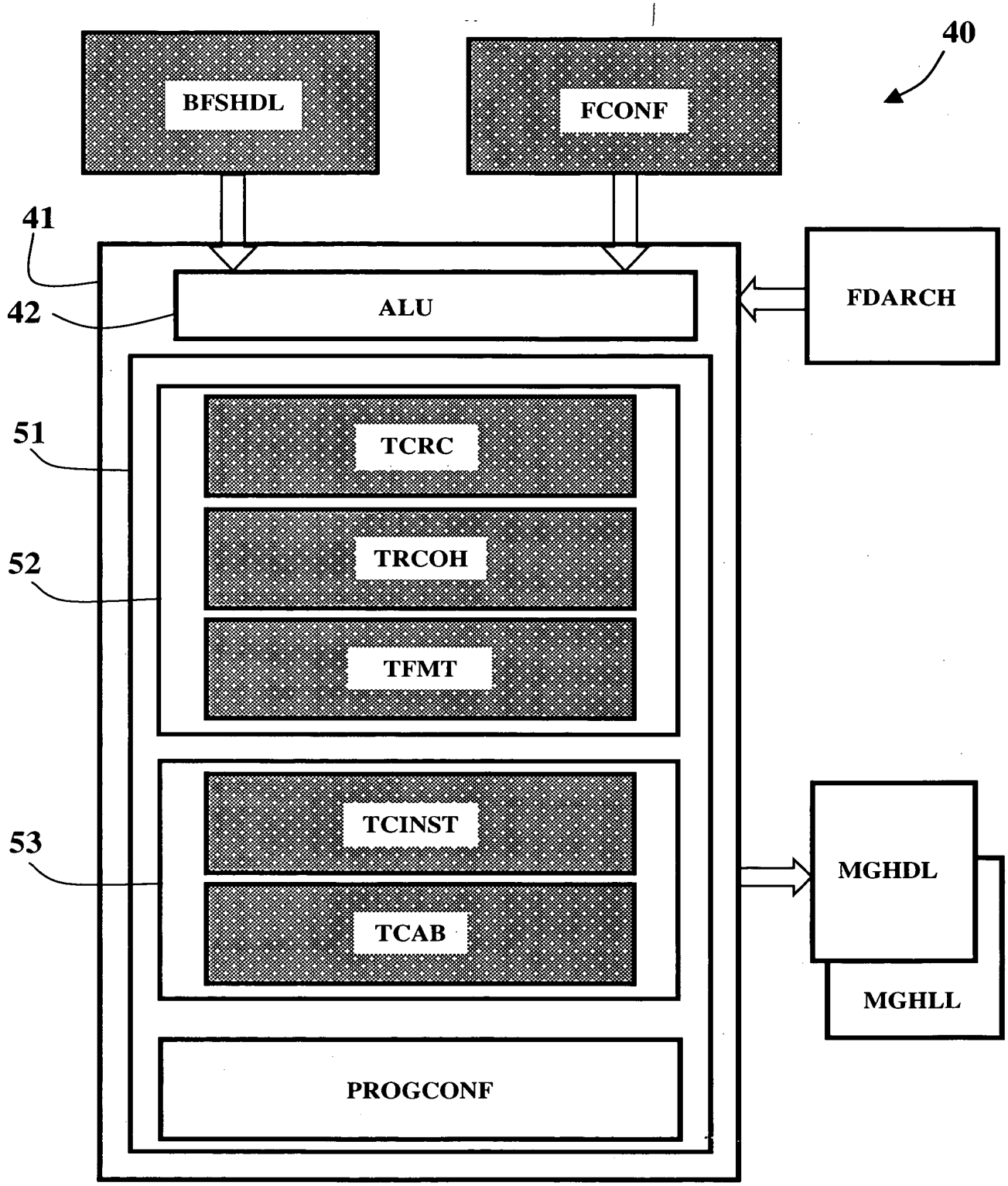
MGHLL
PROGCONF

FIGURE 2B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TRCOH
TFMT
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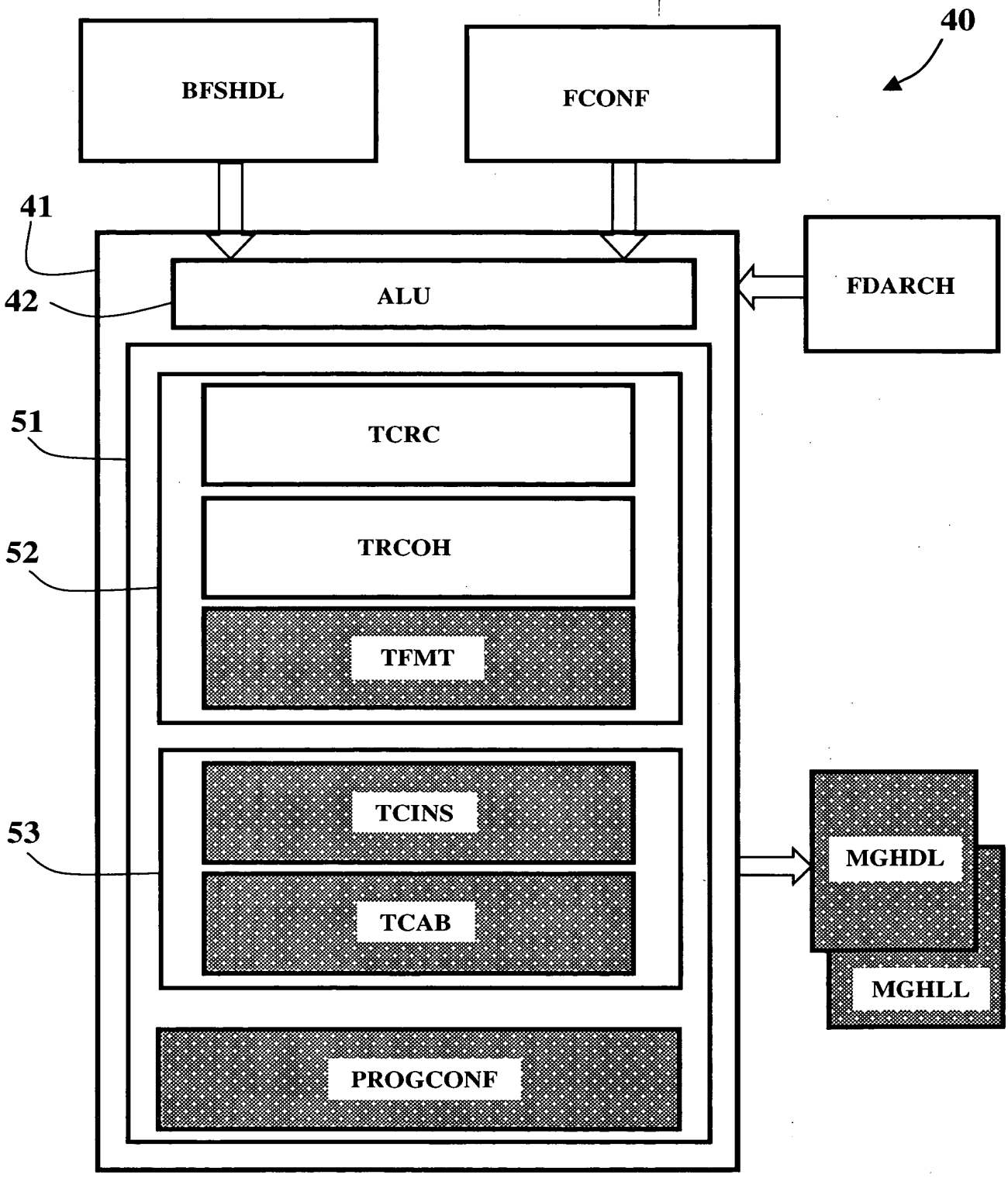
TCINST
TCAB
MGHDL
MGHLL
PROGCONF

FIGURE 2C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FCONF
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FDARCH
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TCRC
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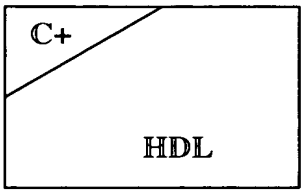
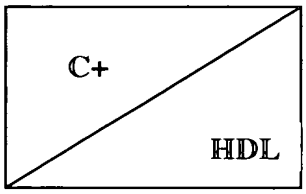
TRCOH
TFMT
53
TCINS
TCAB
MGHDL
MGHLL
PROGCONF

FIGURE 2D



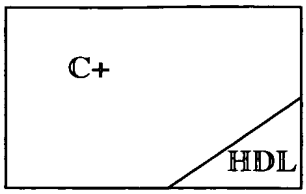
HDL Modeling

Fig. 3a



General case

Fig. 3b



C++ Modeling

Fig. 3c

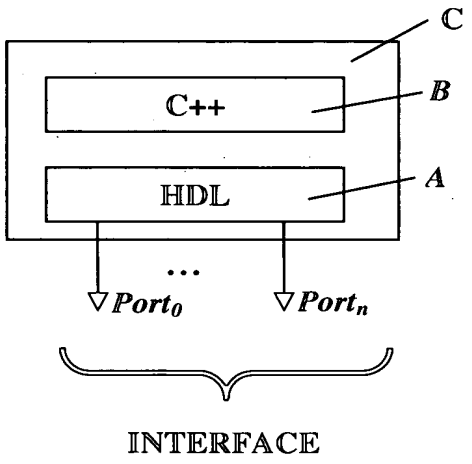


Figure 4 : Generic Structure of an Elementary Model

```
TCRC    %InstNameModuleMap
TCRC    %SysConnectMap
TCRC    %SysSpecMap
TCRC    %SysWrapMap
TCRC    %SysPinConst
TCRC    %Activity_TypeMap
TCRC    %PortProbeMap
TRCOH   %HwfConnectivityMap
TRCOH   %HwifAlternateMap
TFMT    %moduleToCppClassMap
TFMT    %classCppProtoMap
```

Figure 6

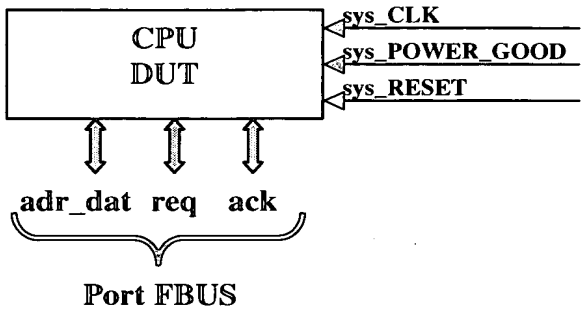


Figure 7a

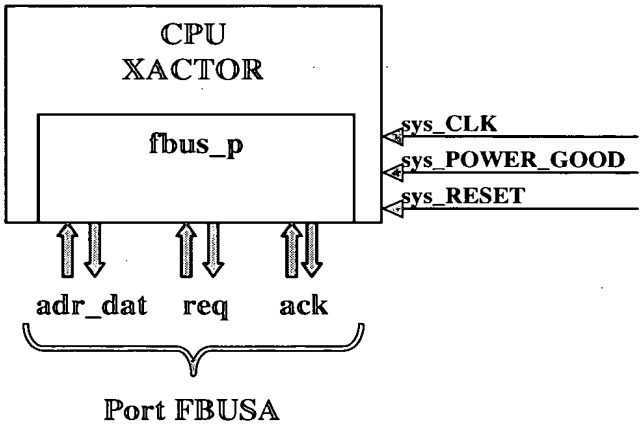


Figure 7b

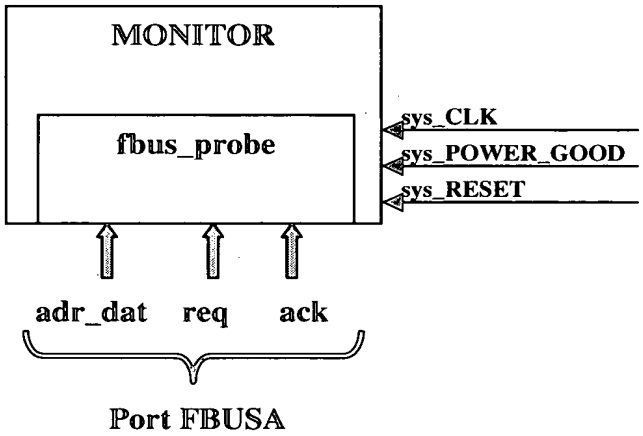


Figure 7c

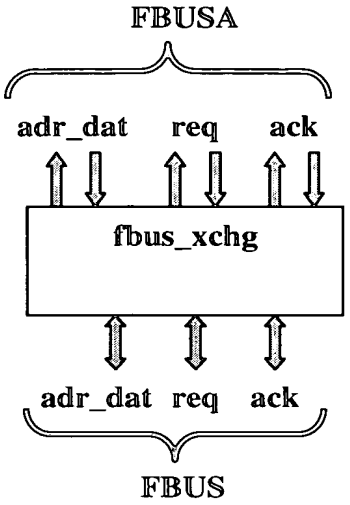


Figure 7e

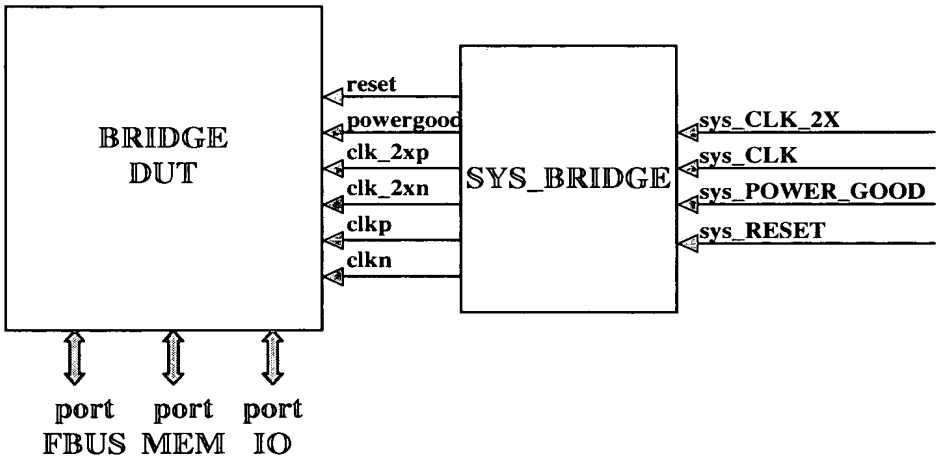


Figure 7e

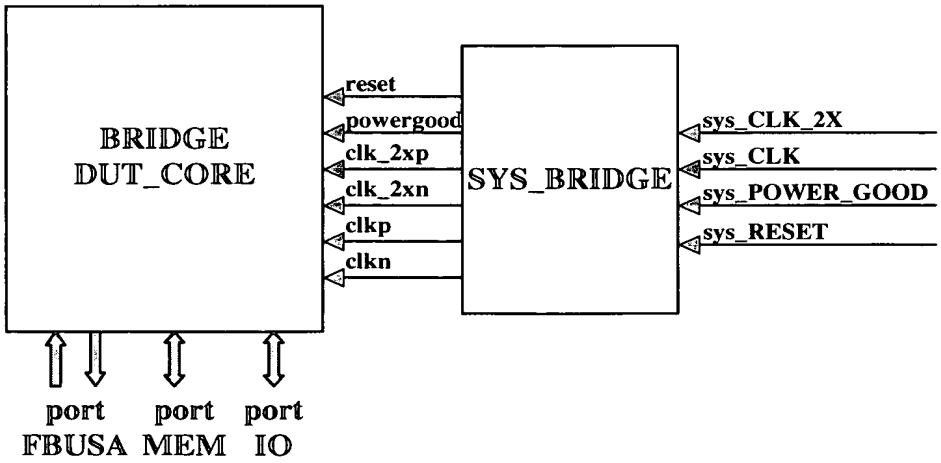


Figure 7f

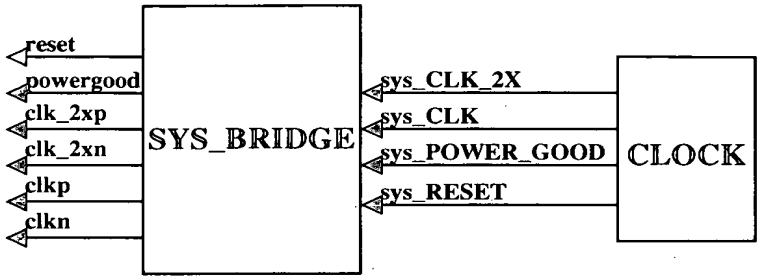


Figure 7g

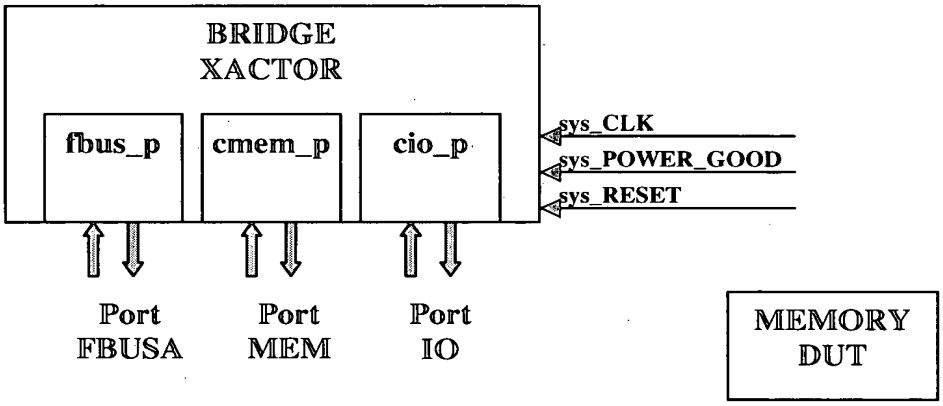


Figure 7h

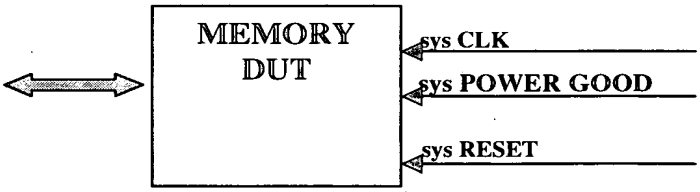


Figure 7i

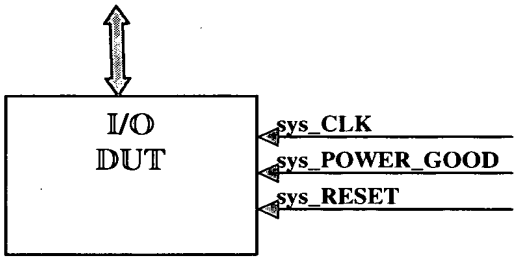


Figure 7j

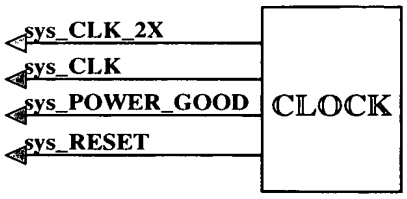


Figure 7k

Figure 8a

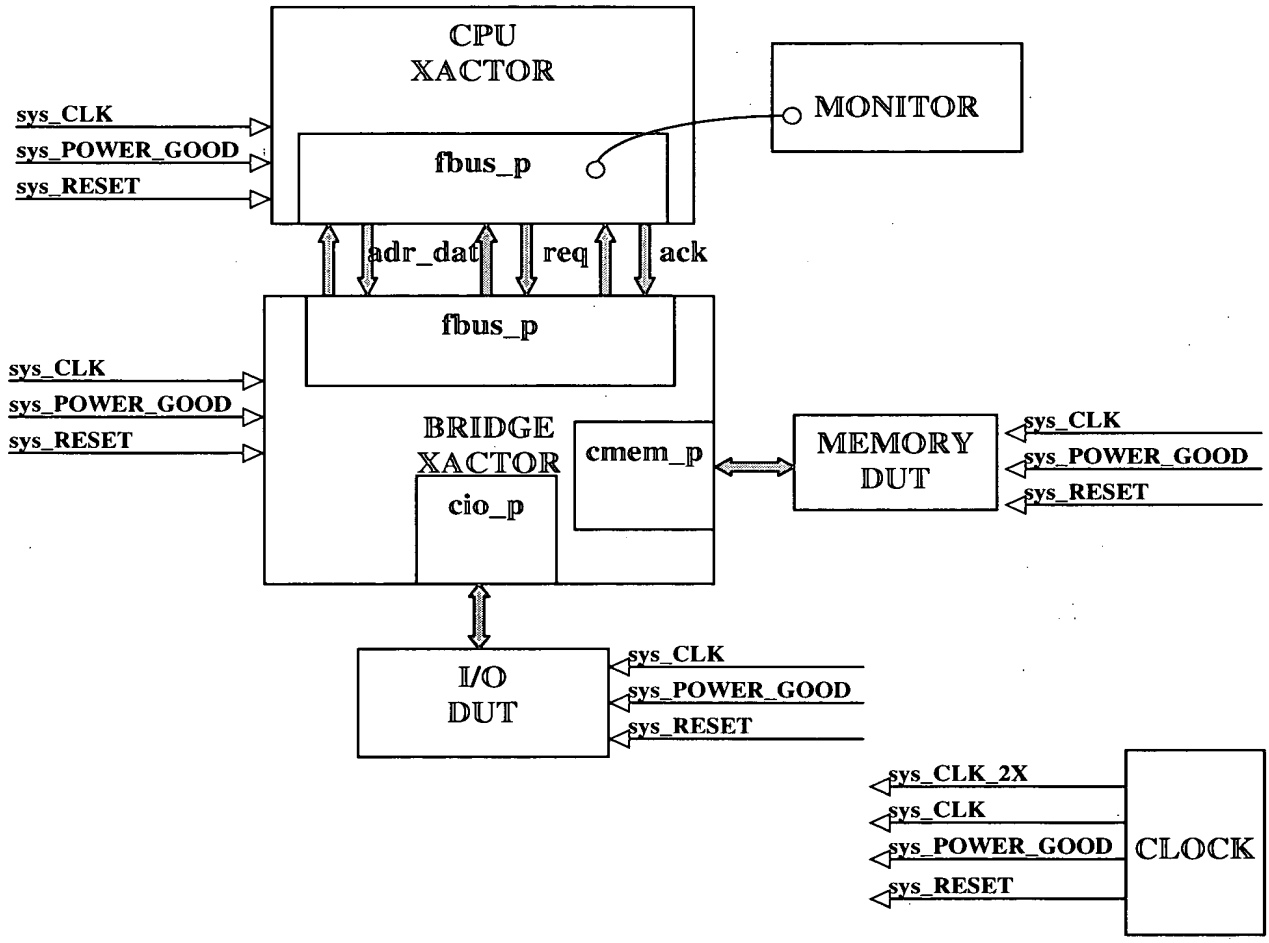
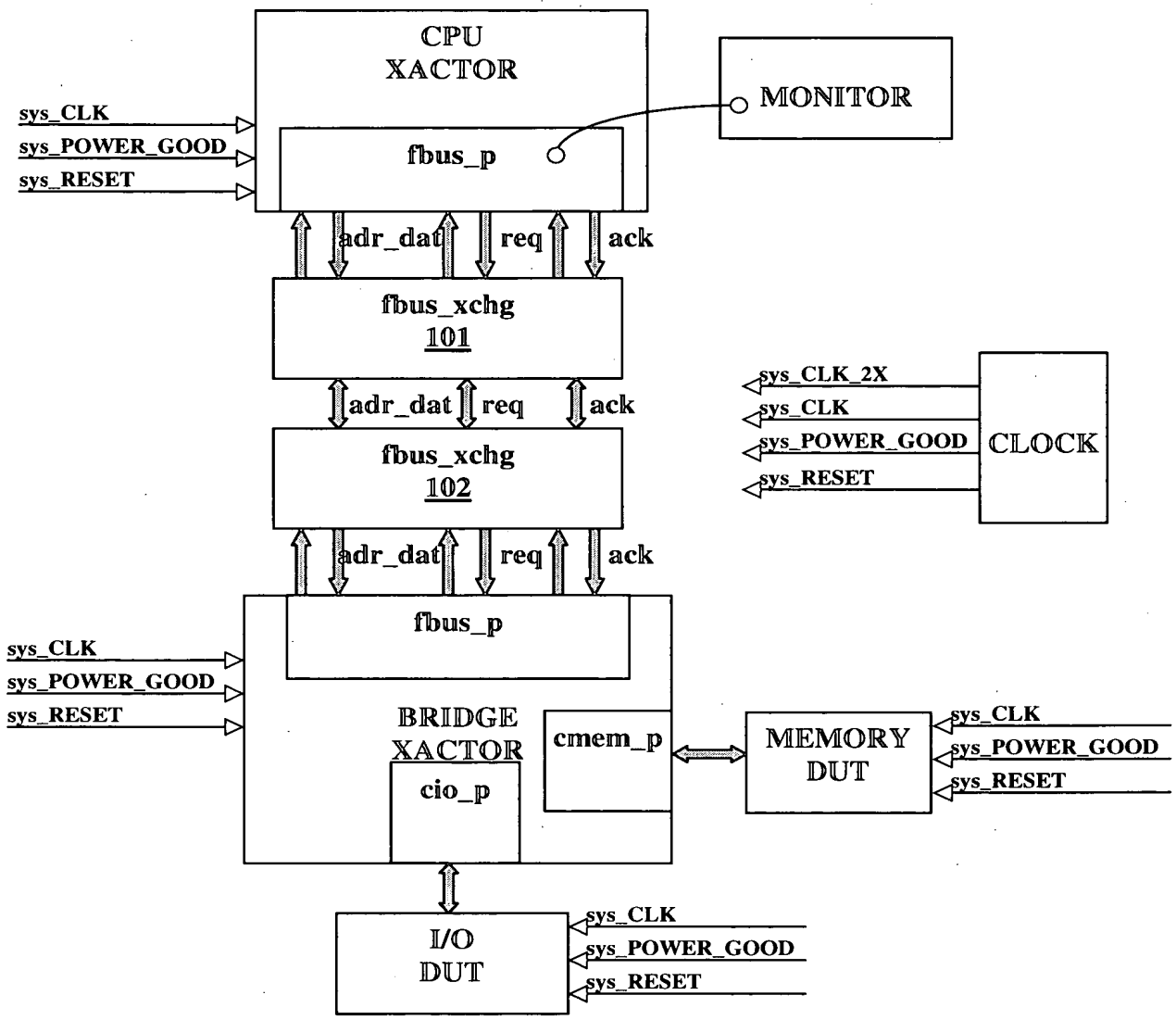

CPU
XACTOR
MONITOR
sys_CLK
sys_POWER_GOOD
sys_RESET
fbus_p
adr_dat
req
ack
fbus_p
sys_CLK
sys_POWER_GOOD
sys_RESET
BRIDGE
XACTOR
cio_p
cmem_p
MEMORY
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET
I/O
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
CLOCK

Figure 8b


CPU
XACTOR
MONITOR
sys_CLK
sys_POWER_GOOD
sys_RESET
fbus_p
adr_dat
req
ack
fbus_xchg
101
fbus_xchg
102
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
CLOCK
fbus_p
BRIDGE
XACTOR
cio_p
cmem_p
MEMORY
DUT
I/O
DUT

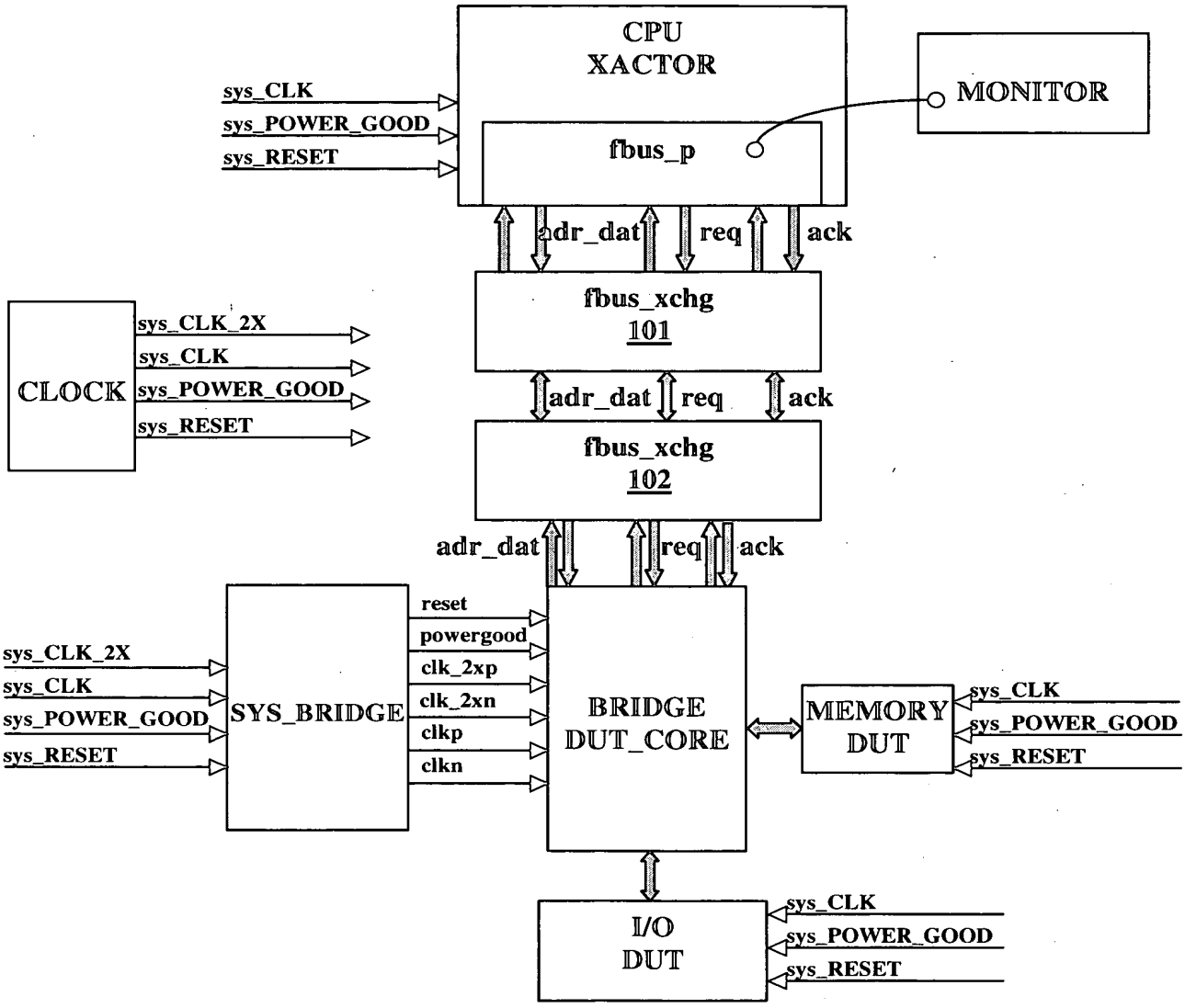

CPU
XACTOR
MONITOR
sys_CLK
sys_POWER_GOOD
sys_RESET
fbus_p
adr_dat
req
ack
fbus_xchg
101
CLOCK
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
adr_dat
req
ack
fbus_xchg
102
adr_dat
req
ack
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
SYS_BRIDGE
reset
powergood
clk_2xp
clk_2xn
clkp
clkn
BRIDGE
DUT_CORE
MEMORY
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET
I/O
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET

Figure 8c

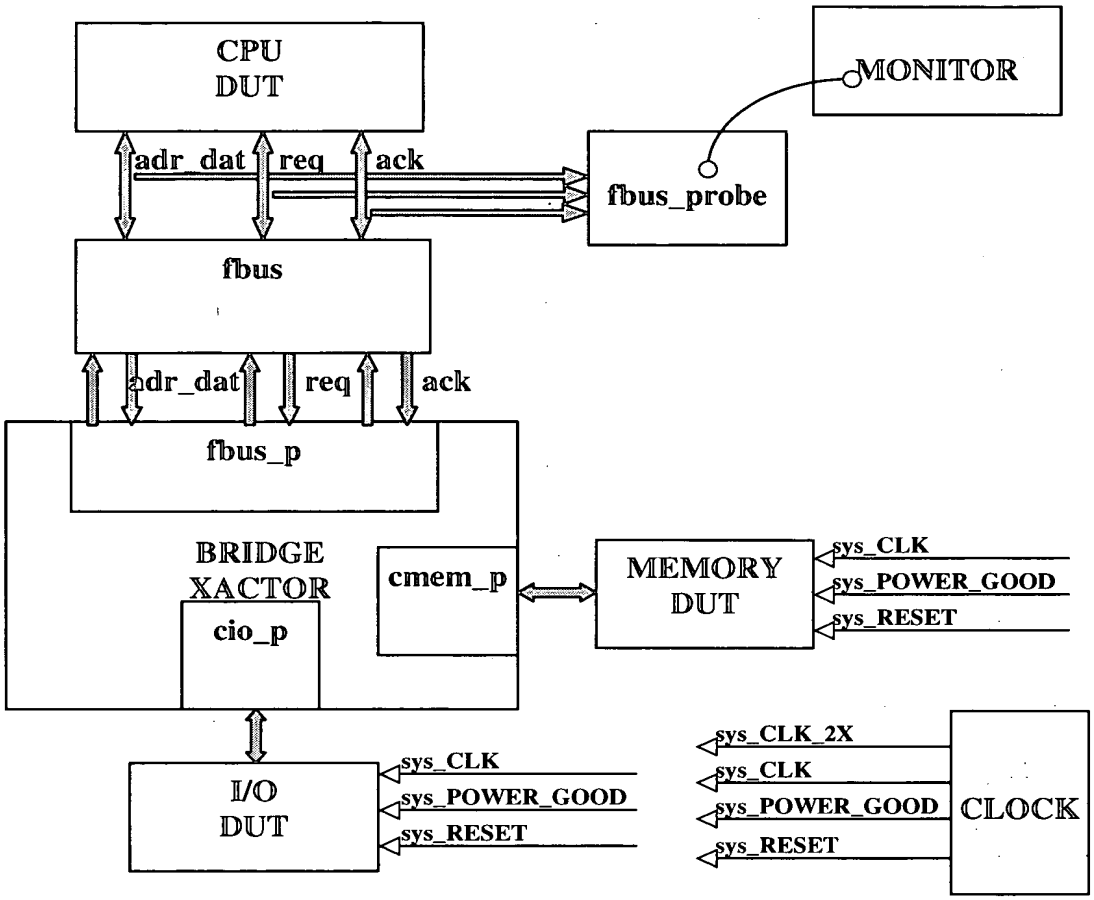

CPU
DUT
MONITOR
adr_dat
req
ack
fbus_probe
fbus
adr_dat
req
ack
fbus_p
BRIDGE
XACTOR
cio_p
cmem_p
MEMORY
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET
I/O
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
CLOCK

Figure 8d

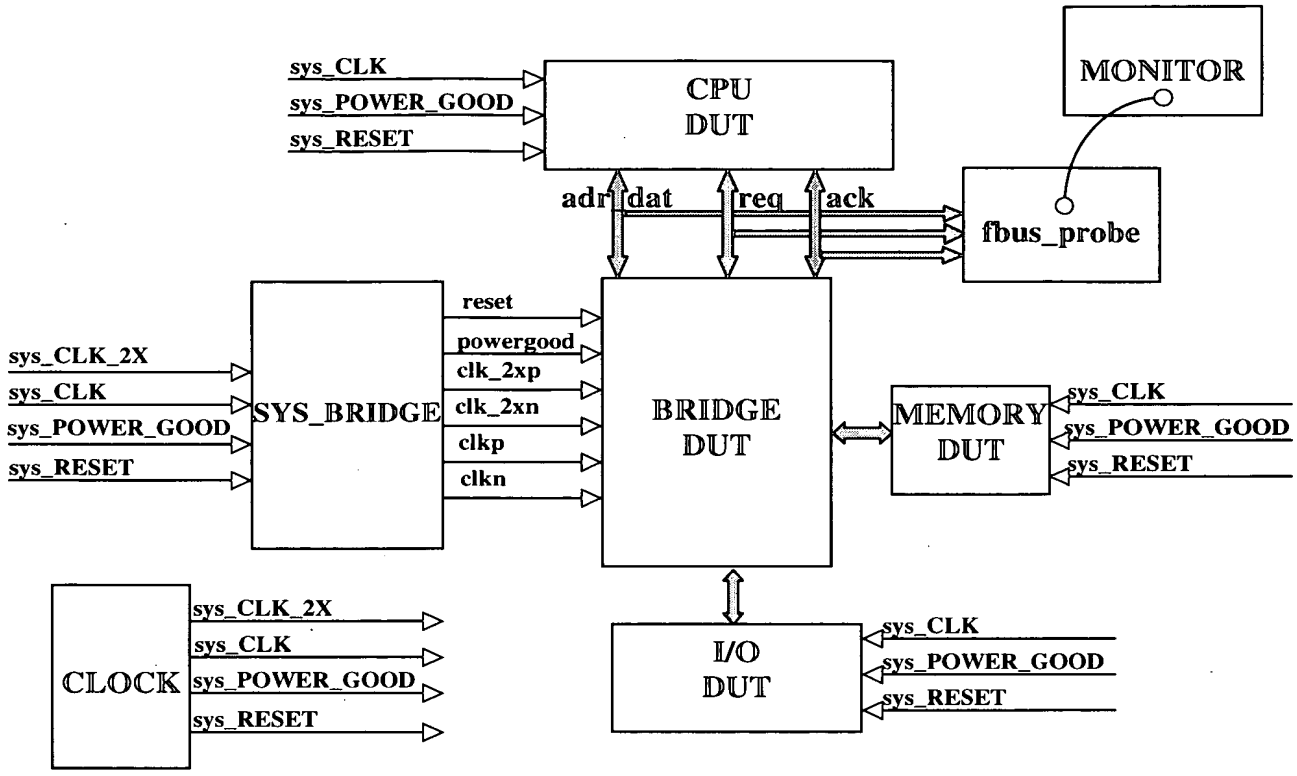
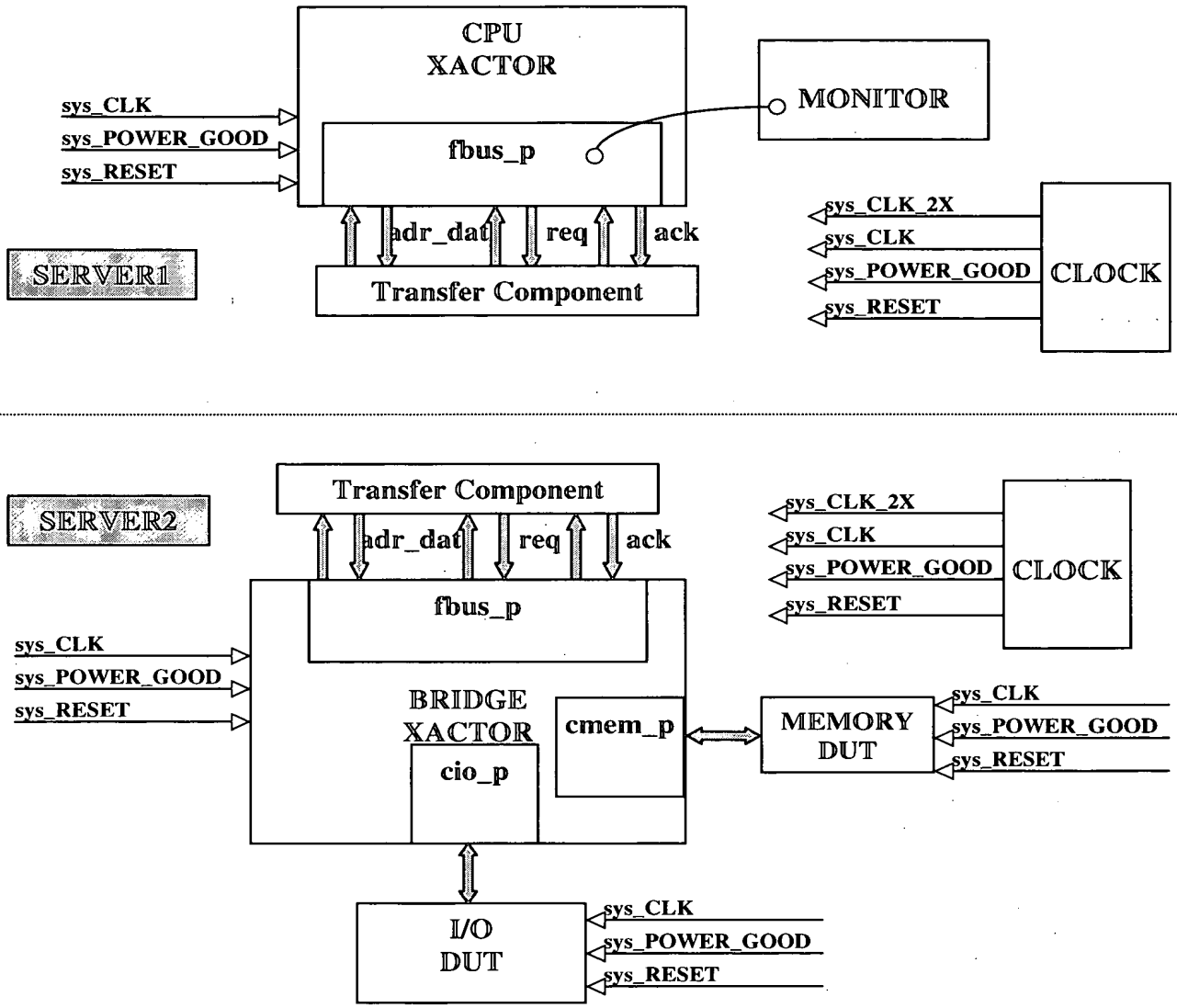

sys_CLK
sys_POWER_GOOD
sys_RESET
CPU
DUT
MONITOR
adr
dat
req
ack
fbus_probe
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
SYS_BRIDGE
reset
powergood
clk_2xp
clk_2xn
clkp
clkn
BRIDGE
DUT
MEMORY
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET
CLOCK
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
I/O
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET

Figure 8e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MONITOR
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sys_POWER_GOOD
sys_RESET
fbus_p
adr_dat
req
ack
SERVER1
Transfer Component
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
CLOCK
Transfer Component
SERVER2
adr_dat
req
ack
fbus_p
sys_CLK_2X
sys_CLK
sys_POWER_GOOD
sys_RESET
CLOCK
sys_CLK
sys_POWER_GOOD
sys_RESET
BRIDGE
XACTOR
cio_p
cmem_p
MEMORY
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET
I/O
DUT
sys_CLK
sys_POWER_GOOD
sys_RESET

Figure 8f